**IN THE CLAIMS:**

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 9-16 and ADD new claims 17-23 in accordance with the following:

Claims 1-16 (cancelled

17. (previously presented) A configuration for digital-analog conversion of a high-frequency digital input signal into a carrier-frequency analog output signal, comprising:

a delay device having at least one delay element, each delay element having an input and an output, the input of a first delay element receiving the high-frequency digital input signal and any additional delay elements connected downstream from the first delay element in a serially consecutive manner;

a first D/A converter having an input receiving the high-frequency digital input signal; and

at least one subsequent D/A converter, each having an input connected to the output of a corresponding delay element, all D/A converters controlled with an identical clock signal and having outputs with a multiple pulse sequence combined in a step-by-step manner to form the analog output signal, where a filter characteristic is realized by assigning specific coefficients to the first and at least one subsequent D/A converters, respectively, and a specific delay time to each delay element, for a total delay time corresponding to at least part of a clock period of the identical clock signal such that the filter characteristic is automatically adjusted if there is a change in carrier frequency range of the output signal, thereby improving filter function.

18. (previously presented) A configuration according to claim 17, wherein the specific coefficients and the specific delay time of each delay element are selected to realize a Finite Impulse Response filter characteristic.

19. (previously presented) A configuration according to claim 18, wherein each delay element is configured as a D latch timed with the identical clock signal.

20. (previously presented) A configuration according to claim 19, wherein all D/A

converters are configured as l-bit D/A converters.

21. (previously presented) A configuration according to claim 20, further comprising adding devices connected to the outputs of all D/A converters for combining thereof.

22. (previously presented) A configuration according to claim 21, wherein the specific delay time assigned to each delay element is identical.

23. (previously presented) A configuration according to claim 22, wherein the high-frequency digital input signal is broadband.